

**DECLARATION**

**SOLE/JOINT INVENTOR  
ORIGINAL/SUBSTITUTE/CIP**

As a below named inventor, I hereby declare that: my residence, post office address, and citizenship are as stated below next to my name. I believe I am the original, first, and sole inventor (if only one name is listed below) or a joint inventor (if plural inventors are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

MEMORY CELL ARRAYS

as described in the specification ☒ attached or ☐ of patent Application Serial No.                     , filed         
                     and amended on                     .

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above; that I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application; that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representative or assigns more than twelve months prior to this application; and that I acknowledge the duty to disclose information of which I am aware which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations § 1.56(a). Such information is material when it is not cumulative to information already of record or being made of record in the application, and

- (1) it establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or
- (2) it refutes, or is inconsistent with, a position the applicant has taken or may take in:
- (i) opposing an argument of unpatentability relied on by the Office, or
  - (ii) asserting an argument of patentability.

I hereby claim foreign priority benefits under Title 35, United States Code § 119 of any foreign application(s) for patent or inventor's certificates listed below and have also identified below any foreign application(s) having a filing date before that of the application(s) on which priority is claimed:

COUNTRY	APPLICATION NUMBER	DATE OF FILING	PRIORITY CLAIMED UNDER 35 USC 119
			<input type="checkbox"/> YES <input type="checkbox"/> NO

I hereby claim the benefit under Title 35 United States Code § 120 of any United States application(s) listed below and, insofar as any subject matter of any claim of this application is not disclosed in the prior United States Application, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations § 1.56(a) which occurred between the filing date of the prior application and the national PCT international filing date of this application:

Serial No.: 08/918,657, entitled "Processing Methods of Forming Integrated Circuitry Memory Devices, Methods of Forming DRAM Arrays, and Related Semiconductor Masks", Filed August 22, 1997

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

FULL NAME OF SOLE OR FIRST INVENTOR LUAN TRAN	INVENTOR'S SIGNATURE <i>Luan Tran</i>	DATE: June 2 <sup>nd</sup> 1999
RESIDENCE 1125 W. SANDY COURT, MERIDIAN, ID 83642		CITIZENSHIP United States
POST OFFICE ADDRESS 1125 W. SANDY COURT, MERIDIAN, ID 83642		
FULL NAME OF SECOND JOINT INVENTOR D. MARK DURCAN	INVENTOR'S SIGNATURE <i>DM Durcan</i>	DATE: June 2 <sup>nd</sup> 1999
RESIDENCE 4850 BOISE RIVER LANE, BOISE, ID 83706		CITIZENSHIP United States
POST OFFICE ADDRESS 4850 BOISE RIVER LANE, BOISE, ID 83706		
FULL NAME OF THIRD JOINT INVENTOR TYLER A. LOWREY	INVENTOR'S SIGNATURE	DATE:
RESIDENCE 2599 EAST PLATEAU DRIVE, BOISE, ID 83712		CITIZENSHIP United States
POST OFFICE ADDRESS 2599 EAST PLATEAU DRIVE, BOISE, ID 83712		
FULL NAME OF FOURTH JOINT INVENTOR ROB B. KERR	INVENTOR'S SIGNATURE <i>Rob B. Kerr</i>	DATE: 6-2-1999
RESIDENCE 2089 E. BONVIEW DRIVE, BOISE, ID 83712		CITIZENSHIP United States
POST OFFICE ADDRESS 2089 E. BONVIEW DRIVE, BOISE, ID 83712		
FULL NAME OF FIFTH JOINT INVENTOR KRIS K. BROWN	INVENTOR'S SIGNATURE <i>Kris K. Brown</i>	DATE: June 2 <sup>nd</sup> 1999
RESIDENCE 8610 W. ATWATER, GARDEN CITY, ID 83714		CITIZENSHIP United States
POST OFFICE ADDRESS 8610 W. ATWATER, GARDEN CITY, ID 83714		

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MEMORY CELL ARRAYS

as described in the specification [X] attached or [ ] of patent Application Serial No.                     , filed         
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FULL NAME OF SECOND JOINT INVENTOR D. MARK DUNCAN	INVENTOR'S SIGNATURE	DATE:
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POST OFFICE ADDRESS 4850 BOISE RIVER LANE, BOISE, ID 83706		
FULL NAME OF THIRD JOINT INVENTOR TYLER A. LOWREY	INVENTOR'S SIGNATURE <i>Tyler A. Lowrey</i>	DATE: 6/17/99
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POST OFFICE ADDRESS 2599 EAST PLATEAU DRIVE, BOISE, ID 83712		
FULL NAME OF FOURTH JOINT INVENTOR ROB B. KERR	INVENTOR'S SIGNATURE	DATE:
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POST OFFICE ADDRESS 8610 W. ATWATER, GARDEN CITY, ID 83714		

[illegible]

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The undersigned is authorized to sign this statement on behalf of the Assignee.

Please direct all communications to: TROP, PRUNER, HU & MILES, 8554 Katy Freeway, Suite 100, Houston, Texas 77024 to the attention of: Timothy N. Trop, telephone number (713) 468-8880.

**ASSIGNEE**  
MICRON TECHNOLOGY, INC.

Date: Jun 24, 1999

BY:   
NAME: Michael L. Lynch

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